

Sampling signal generating circuit for sampling apparatus and digital oscilloscope

Patent Number:  [US5914592](#)
Publication date: 1999-06-22
Inventor(s): SAITO MASANORI (JP)
Applicant(s): HITACHI ELECTRONICS (JP)
Requested Patent:  [JP8220144](#)
Application Number: US19960597407 19960208
Priority Number(s): JP19950022603 19950210
IPC Classification: G01R13/34
EC Classification: [G01R13/34](#)
Equivalents: JP3311889B2

Abstract

A signal from an original oscillation circuit is inputted into a phase-locked loop circuit capable of continuously varying a frequency of this signal derived from the original oscillation circuit. The phase-locked loop circuit changes the frequency of the signal derived from the original oscillation circuit into another frequency corresponding to sweep rate variable information derived from a sampling control unit, and then outputs the signal having the changed frequency. This signal outputted from the phase-locked loop circuit is supplied to a variable frequency dividing circuit. This variable frequency dividing circuit frequency-divides the frequency of the signal outputted from the phase-locked loop circuit at an arbitrary frequency dividing ratio corresponding to the sweep rate range information given from the sampling control unit, and thereafter outputs the signal with the frequency-divided frequency as a sampling signal.

Data supplied from the esp@cenet database - I2